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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,577	MOYER, WILLIAM C.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,9,10 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,10 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 and 9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Spiller, US Patent 6,047,122 (herein referred to as Spiller).

3. Referring to claim 1, Spiller has taught a method for a processor, having a register file comprising a plurality of registers (The processor, element 200, contains a register file where data operands from the control network interface are transmitted and stored. Elements 855, 860, and 863 also comprise the register file.) and a broadcast specifier corresponding to the register file (Elements 850, 851, and 852 contain the broadcast specifiers. See Figure 7B-2A), to selectively broadcast via a coprocessor communication bus, write transactions to said register file (column 45, line 27-column 59, line 42, Data is selectively transmitted to processor 200 based on elements 850, 851, and 852, through registers 855, 860, and 863.), the method comprising:

a. receiving an operand to be written to said register file (Operands to be written to the processor are received by the FIFO's, elements 833-835, and elements 855, 860 and 863 .);

b. selecting one of said plurality of registers in said register file (column 45, line 27-column 59, line 42);

c. providing to said register file said operand to be written to said register file (column 45, line 27-column 59, line 42, Data is provided to elements 855, 860 and 863 and then written to the processor register file.); and

d. selectively providing via said coprocessor communication bus said operand to be written in said register file based on the broadcast specifier (855, 860 and 863), wherein said operand is provided to said coprocessor communication bus when the broadcast specifier indicates that broadcasting is enabled and said operand is not provided to said coprocessor communication bus when the broadcast specifier indicates that broadcasting is not enabled (column 45, line 27-column 59, line 42, The broadcast specifiers enable an operand to be provided to the register file of the processor, through a coprocessor communication bus, by asserting a POP signal. The broadcast specifiers do not allow an operand to be provided to the register file of the processor, through a coprocessor communication bus, by inhibiting a POP signal from being enabled.).

4. Referring to claim 2, Spiller has taught the method of claim 1, as described above, and wherein the broadcast specifier comprises a set of broadcast indicators, each broadcast indicator within the set of broadcast indicators corresponding to one of the plurality of registers (Elements 850, 851, and 852 comprise the set of broadcast indicators. Element 850 corresponds to elements 834 and 855. Element 851 corresponds to elements 833 and 860. Element 852 corresponds to elements 835 and 863.).

5. Referring to claim 3, Spiller has taught the method of claim 2, as described above, and wherein selectively providing via said coprocessor communication bus said operand to be written in said register file is based on the broadcast indicator corresponding to the selected one of said

plurality of registers in said register file (column 45, line 27-column 59, line 42, The broadcast specifiers enable an operand to be provided to the register file of the processor, through a coprocessor communication bus, by asserting a POP signal. The broadcast specifiers do not allow an operand to be provided to the register file of the processor, through a coprocessor communication bus, by inhibiting a POP signal from being enabled.).

6. Referring to claim 4, Spiller has taught the method of claim 1, as described above, and wherein the broadcast specifier is one of a plurality of broadcast specifiers within the processor, each of the plurality of broadcast specifiers corresponding to at least one broadcast region of the processor (Element 850 corresponds to broadcast region 834, element 851 corresponds to broadcast region 833, and element 852 corresponds to broadcast region 835.).

7. Referring to claim 5, Spiller has taught a the method of claim 4, as described above, and further comprising:

a. selectively providing, via said coprocessor communication bus, a region indicator corresponding to a current broadcast region of a current write transaction (column 45, line 27-column 59, line 42, "SBC", "BC" and "COM" indicate the broadcast regions.).

8. Referring to claim 9, Spiller has taught a method for a processor, having a register file comprising a plurality of registers (The processor, element 200, contains a register file where data operands from the control network interface are transmitted and stored. Elements 855, 860, and 863 also comprise the register file.), to selectively broadcast via a coprocessor communication bus, write transactions to said register file (column 45, line 27-column 59, line 42, Data is selectively transmitted to processor 200 based on elements 850, 851, and 852, through registers 855, 860, and 863.), the method comprising:

a. receiving an operand to be written to said register file (Operands to be written to the processor are received by the FIFO's, elements 833-835, and elements 855, 860 and 863 .);

b. selecting one of said plurality of registers in said register file (column 45, line 27-column 59, line 42);

c. providing to said register file said operand to be written to said register file (column 45, line 27-column 59, line 42, Data is provided to elements 855, 860 and 863 and then written to the processor register file.); and selectively

d. providing via said coprocessor communication bus said operand to be written in said register file based on a current execution region of said processor (column 45, line 27-column 59, line 42, elements 833-835 , "SBC", "BC" and "COM" indicate the execution regions.), wherein selectively providing comprises:

i. determining whether broadcast is enabled for the current execution region, and if broadcast is enabled for the current execution region, providing said operand via said coprocessor communication bus, and if broadcast is not enabled for the current execution region, not providing said operand via said coprocessor communication bus (column 45, line 27-column 59, line 42, Elements 850, 851, and 852 determine whether broadcast is enabled for the current execution region. If broadcast is enabled for the current execution region, then an operand is provided to the register file of the processor, through a coprocessor communication bus, by asserting a POP signal for the current execution region. If

broadcast is not enabled for the current execution region, then a POP signal for the current execution region is not asserted.).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 10 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al., US Patent 6,138,185 (herein referred to as Nelson).

11. Referring to claim 10, Nelson has taught a processor, comprising:

a. a plurality of registers (In storage systems and workstations as described in the reasoning below.);

b. circuitry for performing a write operation to one of the plurality of registers (Figure 6, column 1, lines 10-30 and lines 42-54, column 3, lines 36-46, column 4, lines 17-30);

c. conductors for providing an operand for the write operation to said one of the plurality of registers (Figure 6, column 1, lines 10-30 and lines 42-54, column 3, lines 36-46, column 4, lines 17-30);

d. a set of broadcast specifiers, each broadcast specifier within the set of broadcast specifiers comprising a set of broadcast indicators wherein each broadcast indicator corresponds to a register of the plurality of registers and indicates whether or not a write to the corresponding register is to be broadcasted (column 8, line 25-column9, line 19,

Each group is associated with a separate entry, element 601. Element 601 contains a plurality of enable bits, or broadcast indicators. The broadcast indicators determine whether to broadcast to the corresponding destination locations.);

e. compare circuitry for comparing the one of the plurality of registers and a corresponding broadcast indicator within a selected one of the broadcast specifiers and for providing a broadcast enable signal, wherein the broadcast enable signal enables broadcasting when the corresponding broadcast indicator indicates broadcasting for the one of the plurality of registers and the broadcast signal does not enable broadcasting when the corresponding broadcast indicator does not indicate broadcasting for the one of the plurality of registers (column 8, line 25-column9, line 19, The group definition bits, i.e. element 602, and the enable bits, element 601, are compared to determine which bits in a particular group are to be broadcasted.); and

f. a port coupled to the compare circuitry for communicating with a coprocessor communication bus, said port comprising at least one coprocessor communication bus signal for providing said operand when said broadcast enable signal enables broadcasting and not providing said operand when said broadcast enable signal does not enable broadcasting (column 8, line 25-column9, line 19, Data operands are broadcast when they are in the group, defined by element 602, and when they are enabled by element 601.).

g. Nelson has not specifically taught a plurality of registers. However, Nelson has taught that the switch of Figure 2 interconnects data for point-to-point communications between servers, storage systems, workstations, switches, and hubs. (Column 1, lines 10-17, and lines 42-55.). However, using registers to store operand data is well known in

storage systems and in processors in workstations for high speed access to the data. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the storage of data in Nelson, be stored in registers, for the desirable purpose of high speed access to the data operands.

12. Referring to claim 13, Nelson has taught the processor of claim 10, as described above, and further comprising:

a. a program counter unit, for indicating address locations; and a broadcast region control unit, coupled to the program counter unit, for indicating when the indicated address location from the program counter unit falls within one of a set of broadcast regions (column 8, line 25-column9, line 19, Figure 4, An address D0-D7 is indicated being between 0xF0 and 0xFF.).

13. Referring to claim 14, Nelson has taught the processor of claim 13, as described above, and wherein the port further comprises at least one coprocessor communication bus signal indicating a current broadcast region from the set of broadcast regions when the indicated address location falls within one of the set of broadcast regions (Figure 4, element 205b, column 8, line 25-column9, line 19, Broadcast regions are 0xF0 to 0xFF.).

14. Referring to claim 15, Nelson has taught the processor of claim 13, as described above, and wherein the broadcast region control unit comprises a plurality of region storage devices, wherein each broadcast region within the set of broadcast regions has a corresponding region storage device (Figure 6, column 8, line 25-column9, line 19).

15. Referring to claim 16, Nelson has taught the processor of claim 15, as described above, and wherein each region storage device comprises an upper bound storage device and a lower

bound storage device to define each broadcast region (column 8, line 25-column 9, line 19, Bit mask 602 defines each broadcast region, which includes a lower bound and an upper bound storage device to define each region.).

16. Referring to claim 17, Nelson has taught the processor of claim 15, as described above, and wherein each region storage device comprises a base location storage device and a mask storage device to define each broadcast region (column 8, line 25-column 9, line 19, Figure 6).

17. Referring to claim 18, Nelson has taught a processor, comprising:

a. a plurality of registers (In storage systems and workstations as described in the reasoning below.);

b. circuitry for performing a write operation to one of the plurality of registers (Figure 6, column 1, lines 10-30 and lines 42-54, column 3, lines 36-46, column 4, lines 17-30),

c. conductors for providing an operand for the write operation to said one of the plurality of registers (Figure 6, column 1, lines 10-30 and lines 42-54, column 3, lines 36-46, column 4, lines 17-30);

d. a program counter unit for indicating address locations; an execution region control unit, coupled to the program counter unit, for indicating when the indicated address location from the program counter unit falls within one of a set of execution regions (column 8, line 25-column9, line 19, Figure 4, An address D0-D7 is indicated being between 0xF0 and 0xFF.), each execution region indicating a range of instruction addresses (Each region indicates a range of instruction addresses to broadcast to based on group members and the enable bits.), and

e. a port, coupled to the execution region control unit, for communicating with a coprocessor communication bus, said port comprising at least one coprocessor communication bus signal indicating a current execution region from the set of execution regions when the indicated address location falls within one of the set of execution regions (Figure 4, element 205b, column 8, line 25-column9, line 19, Broadcast regions are 0xF0 to 0xFF.).

18. Nelson has not specifically taught a plurality of registers. However, Nelson has taught that the switch of Figure 2 interconnects data for point-to-point communications between servers, storage systems, workstations, switches, and hubs. (Column 1, lines 10-17, and lines 42-55.). However, using registers to store operand data is well known in storage systems and in processors in workstations for high speed access to the data. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the storage of data in Nelson, be stored in registers, for the desirable purpose of high speed access to the data operands.

19. Referring to claim 19, Nelson has taught the processor of claim 18, as described above, and wherein said port further comprises:

a. at least one coprocessor communication bus signal for selectively providing said operand to be written to said one of the plurality of registers during said write operation based on the current execution region (column 8, line 25-column 9, line 19, connect requests).

20. Referring to claim 20, Nelson has taught the processor of claim 18, as described above, and wherein the execution region control unit comprises a plurality of region storage devices,

wherein in each execution region within the set of execution regions has a corresponding region storage device for defining the execution region (Figure 6, column 8, line 25-column 9, line 19).

Response to Arguments

21. Applicant's arguments with respect to claims 1-5, 9, 10, and 13-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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